IN THE CLAIMS:

Kindly amend the claims, as follows:

1. (Currently Amended) A signal processing apparatus comprising:

an input circuit to receive an input signal;

a high-pass filter responsive to said input circuit,

wherein said high-pass filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit ~~directly~~ responsive to said high-pass filter; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

2. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has a low cutoff frequency.

3. (Previously Presented) A signal processing apparatus according to Claim 2, wherein said high-pass filter has a flat response.

4. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequency.

5. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequencies.

6. (Previously Presented) A signal processing apparatus according to Claim 5, wherein the high attenuation is at least 20 db.

7. (Canceled)

~~8.~~ (Currently Amended) ~~A signal processing apparatus according to Claim 7,~~ A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said ~~first~~ FIR filter comprises M taps to filter precursor ~~ISI~~, one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0;

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

~~9.~~ (Currently Amended) A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a ~~first~~ finite impulse response (FIR) filter ~~(FIR)~~,

wherein said ~~first~~ FIR filter comprises M taps to filter precursor ~~ISI~~, one main tap and N taps to filter postcursor ISI,

wherein each tap of said ~~first~~ FIR filter has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$-1 << W_1, \ldots W_n << 0$; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

7 ~~10~~. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said input circuit comprises an analog to digital converter.

8 ~~11~~. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said decision circuit comprises a threshold circuit.

9 ~~12~~. (Previously Presented) A signal processing apparatus according to Claim 1, wherein said decision circuit comprises a Viterbi detector.

14 ~~13~~. (Currently Amended) ~~A signal processing apparatus according to Claim 8, further comprising~~ A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter, and

wherein said FIR filter comprises M taps to filter precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI;

~~a first~~ an adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering postcursor ISI; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

15

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

15 14. (Previously Presented) A signal processing apparatus according to Claim ~~14~~ 14, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

16 18. (Currently Amended) A signal processing apparatus according to Claim ~~13~~ 14, wherein said ~~first~~ adaptive control circuit is operable only during signal acquisition.

10 16. (Currently Amended) A signal processing apparatus according to Claim 1, wherein said feedback filter comprises a ~~second~~ finite impulse response (FIR) filter ~~(FIR)~~.

11 17. (Currently Amended) A signal processing apparatus according to Claim ~~16~~ 10, further comprising ~~a second~~ an adaptive control circuit to adapt taps of said ~~second~~ FIR filter.

17 18. (Currently Amended) A signal processing apparatus comprising:

input means for receiving an input signal;

high-pass filtering means for filtering the input signal received by said input means,

wherein said high-pass filtering means comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means ~~directly~~ responsive to said high-pass filtering means for recovering data from an output of said high-pass filtering means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

16

19. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means has a low cutoff frequency.

20. (Currently Amended) A signal processing apparatus according to Claim 19, wherein said ~~feedforward equalizer~~ high-pass filtering means has a flat response.

21. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means has high attenuation at low frequency.

22. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means has high attenuation at low frequencies.

23. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means shortens a length of postcursor ~~inter-symbol-interference.~~

24. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means attenuates ~~any~~ DC noise.

25. (Currently Amended) A signal processing apparatus according to Claim 18, wherein said ~~feedforward equalizer~~ high-pass filtering means attenuates baseline wander.

26. (Previously Presented) A signal processing apparatus according to Claim 22, wherein the high attenuation is at least 20 db.

27. (Canceled)

31
~~28.~~ (Currently Amended) ~~A signal processing apparatus according to Claim 27,~~ A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said ~~first~~ FIR filter means comprises M taps for filtering precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

32
~~29.~~ (Currently Amended) A signal processing apparatus, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a ~~first~~ finite impulse response (FIR) filter ~~(FIR)~~ means for filtering the input signal,

wherein said ~~first~~ FIR filter means comprises M taps for filtering precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI,

wherein each tap of said ~~first~~ FIR filter means has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$-1<<W_1, \ldots W_n<<0$; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

~~30.~~ (Previously Presented) A signal processing apparatus according to Claim ~~18,~~ wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

~~31.~~ (Previously Presented) A signal processing apparatus according to Claim ~~18,~~ wherein said decision means comprises a threshold circuit.

~~32.~~ (Previously Presented) A signal processing apparatus according to Claim ~~18,~~ wherein said decision means comprises a Viterbi detector.

33. (Currently Amended) ~~A signal processing apparatus according to Claim 28, further comprising~~ A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal, and

wherein said FIR filter means comprises M taps for filtering precursor ~~ISI,~~ one main tap and N taps for filtering postcursor ISI;

~~a first~~ an adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering postcursor ISI; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward

equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

34. (Previously Presented) A signal processing apparatus according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

35. (Currently Amended) A signal processing apparatus according to Claim 33, wherein said ~~first~~ adaptive control means is operable only during signal acquisition.

~~36.~~ 29 (Currently Amended) A signal processing apparatus according to Claim ~~18,~~ 13 wherein said feedback filter means comprises a ~~second~~ finite impulse response (FIR) filter ~~(FIR)~~ means for filtering the output of said decision means.

~~37.~~ 30 (Currently Amended) A signal processing apparatus according to Claim ~~36,~~ 29 further comprising ~~a second~~ an adaptive control means for adapting taps of said ~~second~~ FIR filter means.

~~38.~~ 36 (Currently Amended) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a high-pass filter responsive to said input circuit,

wherein said high-pass filter comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit directly responsive to said high-pass filter; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

~~39~~ 37. (Original) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said high-pass filter has a low cutoff frequency.

~~40~~ 38. (Original) An Ethernet transceiver according to Claim ~~39~~ 37, wherein said high-pass filter has a flat response.

~~41~~ 39. (Original) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said high-pass filter has high attenuation at low frequency.

~~42~~ 40. (Original) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said high-pass filter has high attenuation at low frequencies.

~~43~~ 41. (Original) An Ethernet transceiver according to Claim ~~42~~ 40, wherein the high attenuation is at least 20 db.

~~44~~. (Canceled)

~~45~~ 42. (Currently Amended) ~~An Ethernet transceiver according to Claim 44,~~ An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a finite impulse response (FIR) filter,

wherein said ~~first~~ FIR filter comprises M taps to filter precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

46. (Currently Amended) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a ~~first~~ finite impulse response (FIR) filter ~~(FIR)~~,

wherein said ~~first~~ FIR filter comprises M taps to filter precursor ~~ISI~~, one main tap and N taps to filter postcursor ISI,

wherein each tap of said ~~first~~ FIR filter has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \ldots W_n << 0; \text{ and}$$

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

47. (Original) An Ethernet transceiver according to Claim ~~38~~, wherein said input circuit comprises an analog to digital converter.

~~48~~ 43. (Original) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said decision circuit comprises a threshold circuit.

~~49~~ 44. (Original) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said decision circuit comprises a Viterbi detector.

~~50~~ 49. (Currently Amended) ~~An Ethernet transceiver according to Claim 45, further comprising~~ An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a ~~first~~ finite impulse response (FIR) filter, and

wherein said FIR filter comprises M taps to filter precursor intersymbol interference (ISI) ~~ISI~~; one main tap and N taps to filter postcursor ISI;

~~a first~~ an adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering postcursor ISI; and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit,

wherein said decision circuit is responsive to said feedback filter.

~~51~~ 50. (Original) An Ethernet transceiver according to Claim ~~50~~ 49, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

~~52~~ 51. (Currently Amended) An Ethernet transceiver according to Claim ~~50~~ 49, wherein said ~~first~~ adaptive control circuit is operable only during signal acquisition.

~~53.~~ 45 (Currently Amended) An Ethernet transceiver according to Claim ~~38~~ 36, wherein said feedback filter comprises a ~~second~~ finite impulse response (FIR) filter ~~(FIR)~~.

~~54.~~ 46 (Currently Amended) An Ethernet transceiver according to Claim ~~53~~ 45, further comprising ~~a second~~ an adaptive control circuit to adapt taps of said ~~second~~ FIR filter.

~~55.~~ 52 (Currently Amended) An Ethernet transceiver, comprising:

input means for receiving an input signal;

high-pass filtering means for filtering the input signal received by said input means,

wherein said high-pass filtering means comprises M taps to filter precursor intersymbol interference (ISI), one main tap and N taps to filter postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means directly responsive to said high-pass filtering means for recovering data from an output of said high-pass filter means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

~~56.~~ 53 (Currently Amended) An Ethernet transceiver according to Claim ~~55~~ 52, wherein said ~~feedforward equalizer~~ high-pass filtering means has a low cutoff frequency.

~~57.~~ 54 (Currently Amended) An Ethernet transceiver according to Claim ~~56~~ 53, wherein said ~~feedforward equalizer~~ high-pass filtering means has a flat response.

~~58.~~ 55 (Currently Amended) An Ethernet transceiver according to Claim ~~55~~ 52, wherein said ~~feedforward equalizer~~ high-pass filtering means has high attenuation at low frequency.

59. (Currently Amended) An Ethernet transceiver according to Claim 55, wherein said ~~feedforward equalizer~~ high-pass filtering means has high attenuation at low frequencies.

60. (Currently Amended) An Ethernet transceiver according to Claim 55, wherein said ~~feedforward equalizer~~ high-pass filtering means shortens a length of postcursor ~~inter-symbol interferenee~~.

61. (Currently Amended) An Ethernet transceiver according to Claim 55, wherein said ~~feedforward equalizer~~ high-pass filtering means attenuates any DC noise.

62. (Currently Amended) An Ethernet transceiver according to Claim 55, wherein said ~~feedforward equalizer~~ high-pass filtering means attenuates baseline wander.

63. (Original) An Ethernet transceiver according to Claim 59, wherein the high attenuation is at least 20 db.

64. (Canceled)

65. (Currently Amended) ~~An Ethernet transceiver according to Claim 64,~~ An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal,

wherein said ~~first~~ FIR filter means comprises M taps for filtering precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI, and

wherein adaptation of each of said N taps is limited to a range of between -1 and 0; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

66. (Currently Amended) An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a ~~first~~ finite impulse response (FIR) filter ~~(FIR)~~ means for filtering the input signal,

wherein said ~~first~~ FIR filter means comprises M taps for filtering precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI,

wherein each tap of said ~~first~~ FIR filter means has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \ldots W_n << 0; \text{ and}$$

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

67. (Original) An Ethernet transceiver according to Claim ~~55~~ 52, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

~~68~~ 64. (Original) An Ethernet transceiver according to Claim ~~55~~ 52, wherein said decision means comprises a threshold circuit.

~~69~~ 65. (Original) An Ethernet transceiver according to Claim ~~55~~ 52, wherein said decision means comprises a Viterbi detector.

~~70~~ 66. (Currently Amended) ~~An Ethernet transceiver according to Claim 65, further comprising~~ An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a finite impulse response (FIR) filter means for filtering the input signal, and

wherein said FIR filter means comprises M taps for filtering precursor ~~ISI~~ intersymbol interference (ISI), one main tap and N taps for filtering postcursor ISI;

~~a first~~ an adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering postcursor ISI; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means,

wherein said decision means is responsive to said feedback filter means.

~~71~~ 67. (Currently Amended) An Ethernet transceiver according to Claim ~~33~~ ~~70~~ 65, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

~~70~~ 68
~~72.~~ (Currently Amended) An Ethernet transceiver according to Claim ~~70~~, wherein said ~~first~~ adaptive control means is operable only during signal acquisition.

64 52
~~73.~~ (Currently Amended) An Ethernet transceiver according to Claim ~~55~~, wherein said feedback filter means comprises a ~~second~~ finite impulse response (FIR) filter ~~(FIR)~~ means for filtering the output of said decision means.

65 64
~~74.~~ (Currently Amended) An Ethernet transceiver according to Claim ~~73~~, further comprising ~~a second~~ an adaptive control means for adapting taps of said ~~second~~ FIR filter means.

28

B